Visual Software International

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Penetrating New Markets

Penetrating Real markets requires meeting sound economic requirements. *VisiSoft* - A Disruptive Innovation - Opens paths to penetrate huge new markets with CAD on Parallel PCs and meets the speed constraints - ***at huge reductions in cost***.

Calls from top engineers - Justin Rattner - Intel, Chuck Moore - AMD, and Craig Mundie - Microsoft, for a new language, and totally new approach to software for parallel processors, are finally answered.

From Art to Architecture

At the beginning of the Renaissance, builders were given artist's depictions of buildings. There were no measurements nor engineering drawings. Can you imagine building skyscrapers, airliners, or bridges without engineering drawings? But one has to use an engineering approach before it can be appreciated.

At VSI, we can't imagine designing complex software without the VisiSoft CAD system. Based upon CAD tools for electronic design, it contains much more than engineering drawings. The language is easily understood by Application Experts. They can create very complex software, with interactive graphics, on parallel processors, more easily than current approaches for a single processor. But one has to use VisiSoft to appreciate all of the facilities.

Software Theory

The software theory that underlies VisiSoft is based on Shannon's Information Theory. This theory provides a mathematical foundation for putting Software on a scientific basis. Using the property of independence, one can design the best data and communication spaces to support fast parallel processing. It provides dramatic improvements in single processor speeds as well as Processor Utilization Efficiency (PUE) on parallel processors.

Based upon the separation of data from instructions, the "Separation Principle" provides for iconic representation of large hierarchical data and rule structures, leading to the development of easily understood independent software modules.

Architectural Facilities

VisiSoft provides for direct mapping of the inherent parallelism - in systems being built or simulated - into a software architecture of Independent (IND) modules. IND modules are typically large and run independently creating high PUEs, see the website: http://www.visisoft.com/PDF_Files/ShowPosters.pdf . PUEs of 85% to 95% are achieved, yielding speed multipliers of 8 to 10X higher than those with current approaches. But then add another factor of 10 to the single processor speeds we use for comparison. Then add another 10X due to the reduction in machine footprint. Visualization of software architectures supports ease of design of data and communication spaces using large amounts of memory - meeting speed constraints while minimizing processor count.

Run-Time System & VisiSoft Parallel OS

Without a Run-Time System (RTS) that is generated automatically from the development environment architectural information, and VisiSoft Parallel OS (VPOS) - that makes optimal use of this information, allocation of memory and processor resources is folly. But again, one has to witness this directly to appreciate it.

Simplification of Chip Design

VisiSoft handles communications between IND modules, ensuring synchronization between processors, and eliminating concerns for cache coherency. Significant simplification in chip design (e.g., no need for cache coherency) allows more memory per processor - the key to speed.

Experiments That Support The Theory

The requirement for repeatable experiments to do fair comparisons in the software field is clear. This implies measures that fairly assess Time-to-Run, Cost-to-Run, and Time & Cost to Build. VSI has produced experiments that can be repeated by anyone with a small amount of effort. These experiments clearly project that a 32 processor PC can do the work of 300,000 HPC processors when the system is not embarrassingly parallel. Don't believe it. Test it! - Pictures below ==> .

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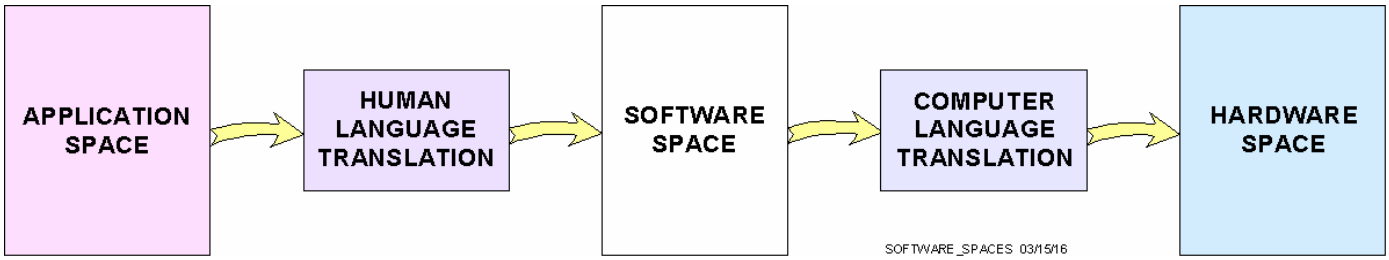
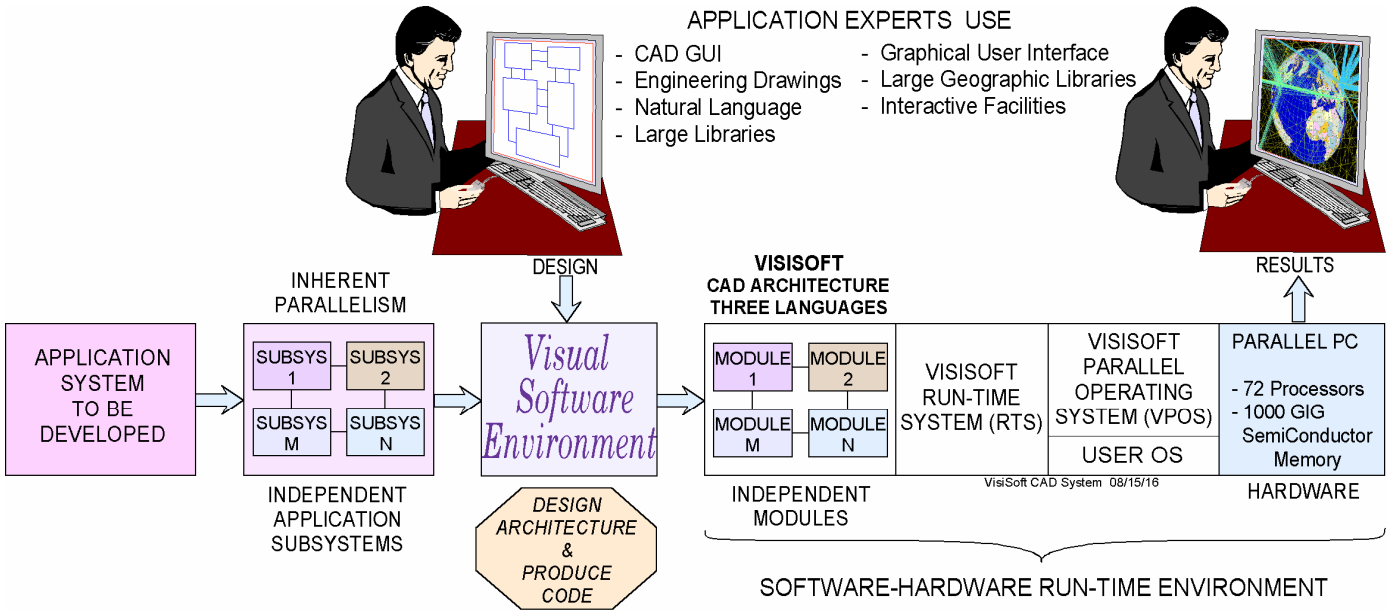
DEVELOPING THE BEST SPACES FOR SPEED AND UNDERSTANDABILITY



Using VisiSoft & the Visual Software Environment (VSE)



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